Avago Technologies Evaluation Board
for Small Form-factor Pluggable (SFP) Transceivers

Application Note 1237

SFP Evaluation Board

The purpose of this Small Form Pluggable (SFP) evaluation board is to provide the designer with a convenient means for evaluating SFP fiber-optic transceivers such as HFBR-5701, HFBR-5710, HFBR-5720, and HFBR-5730 as well as future SFP MSA (Multi-Source Agreement) compatible product offerings. This document describes the details of the evaluation printed circuit board (PCB) and the test equipment and methods for evaluating SFP modules. The detailed operation of the SFP modules and test equipment used with this evaluation PCB are not described in this document, but can be found by obtaining the appropriate documents from the reference section.

Document Outline

I. Equipment List

II. Evaluation PCB Description

III. Electro-Optical Test Configuration(s)

IV. EEPROM Test Configuration

V. Evaluation PCB Schematic

VI. Evaluation PCB Bill of Materials

VII. Reference

I. Equipment List

Included:

1. Evaluation PCB
2. SFP transceiver module(s)

Not Included:

1. 3.3 V DC power supply
2. Fiber optic cables
   - LC to SC
     (1 M and 50/125 μm or 62.5/125 μm)
   - LC to LC Loopback
     (<1 M and 50/125 μm or 62.5/125 μm)
3. 86100A Agilent Digital Communications Analyze (DCA)
4. Agilent Optical/Electrical DCA Plug-In Module 86101A Option H41 or H21 (2125 FC)
5. 86130A Agilent BitAlyzer
   3 Gb/s Bit Error Rate Tester (BERT)
   - Pattern generator, error detector/analyzer
6. Fiber Optic Attenuator (optional)
7. EEPROM reader (optional)
8. PC (optional)

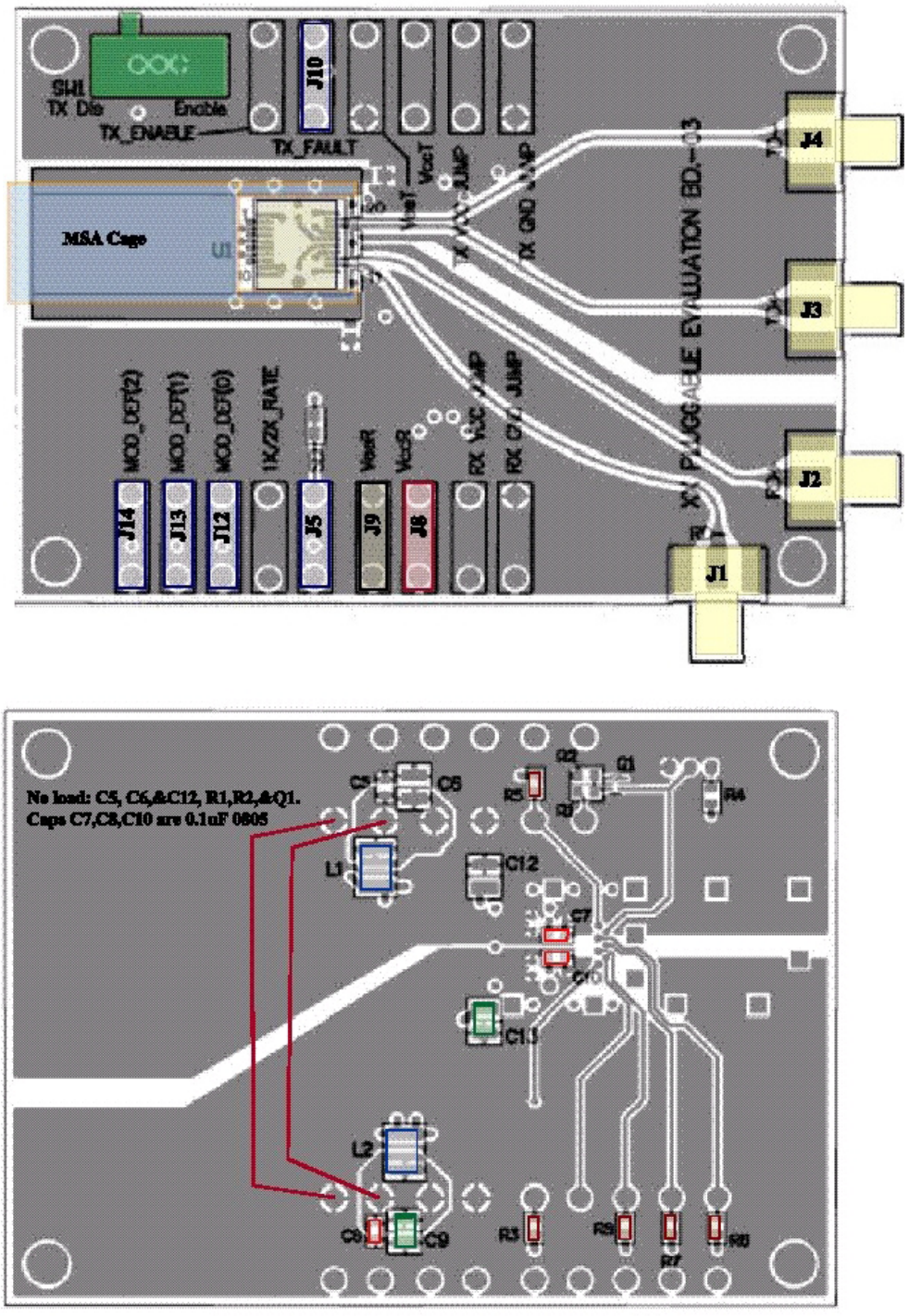

Figure 1. SFP Evaluation Board Top and Bottom View

Table 1. I/O Description

Reference Designator	Name	Description	Signal Level
J1	RD -	Differential receiver outputs	Note 1
J2	RD +		
J3	TD +	Differential transmitter inputs (< 2.4 V)	Note 1
J4	TD -		
J5	SD(LOS)	Signal Detect (LOS) Output: Low indicates sufficient optical power, High indicates insufficient optical power	LVTTL*
J6	VccT	Transmitter Power, no part: jumped to J8	3.3 V
J7	VeeT	Transmitter Ground	GND
J7	VeeT	Transmitter Ground, no part: jumped to J9	GND
J8	VccR	Receiver Power	3.3 V
J9	VeeR	Receiver Ground	GND
J10	TX Fault	Transmitter Fault Output: High output indicates a laser fault, Low indicates normal laser operation	LVTTL*
J12	MOD_DEF (0)	Module Definition 0- grounded by module to indicate that the module is present	LVTTL*
J13	MOD_DEF (1)	Module Definition 1, interfaces to EEPROM. Clock line of serial interface	LVTTL*
J14	MOD_DEF (2)	Module Definition 2, interfaces to EEPROM. Data line of serial interface	LVTTL*
J15	TX VCC JUMP	No Connect, Jump between left and right sides of board implemented with wire on underside.	
J16	TX GND JUMP		
J17	RX VCC JUMP		
J18	RX GND JUMP		
J19	TX_ENABLE	Not Connected, Can be used to electrically to switch TX_DISABLE	
SW1	TX_DISABLE Switch	Transmitter Disable Input: Enable (low signal) enables the transmitter, Disable position (high signal) disables the transmitter.	LVTTL*
U1	SFP Cage Pad	Module plugs here	
	1X/2X Rate	Rate Select Pin, Not Connected	

Notes
1. See specific transceiver data sheet for recommended maximums and further information
* LVTTL defines a 3.3 voltage level with transitions at 0.8 and 2.0 V.

II. Evaluation PCB Description

Top and bottom views of the evaluation PCB are shown in Figure 1. A description of all of the Input/Output (I/O) interfaces on the PCB is shown in Table 1, all of which are found, on the topside of the PCB. The evaluation PCB is a 4-layer design compatible with high-speed signal I/O rates required by 2.125 Gbd Fibre Channel.

III. Electro-Optical Test Configuration(s)

The two basic test configurations for evaluating the SFPs are shown in Figure 2 (Transmitter) and Figure 3 (Receiver or Loopback). These test configurations use one evaluation board and the test instruments from the equipment list, such as a Bit-Error-Ratio Tester (BERT) and a Digital Communication Analyzer (DCA). General considerations about the test configuration follow, but more specific details on SFP transceiver testing can be found in the documents listed in the reference section of this document.

Transmitter Configuration:

This configuration is shown in Figure 2. The SFP's optical characteristics can be tested, including the eye diagram, jitter, and rise/fall time. A representative eye diagram for an SFP is shown in Figure 4. In this configuration, the receiver is not used, however it is recommended that RD- and RD+ be terminated by 50 Ω matched loads. It is also recommended that low loss, low dispersion, and equal length RF cables be used to connect TD+/- to the test equipment.

Receiver Configuration:

This configuration is shown in Figure 3. The SFP's electrical characteristics can be tested, including the receiver electrical eye diagram, jitter, and rise/fall time. A representative eye diagram for an SFP loop back receiver is shown in Figure 5.

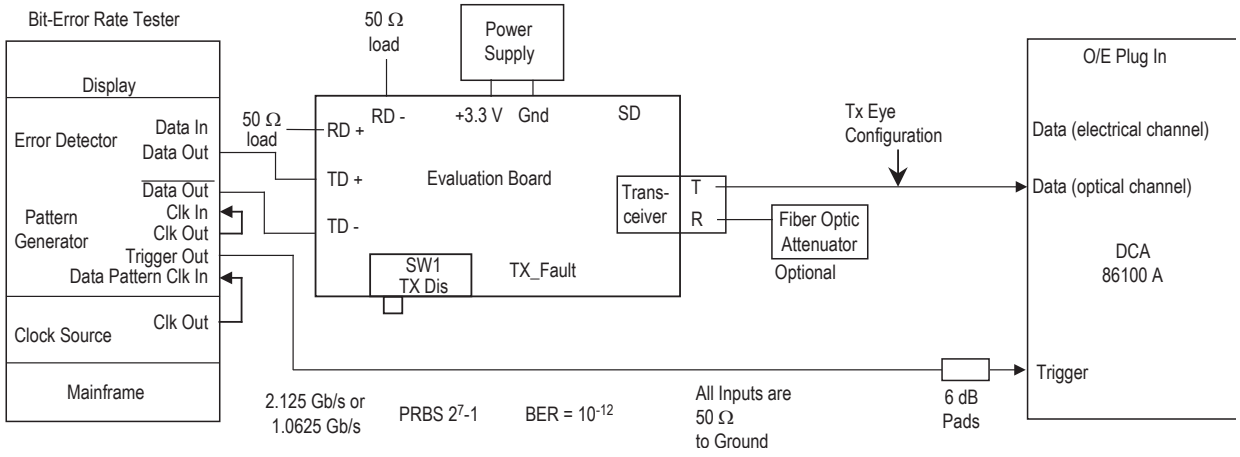

Figure 2. Recommended Transmitter Test Configuration

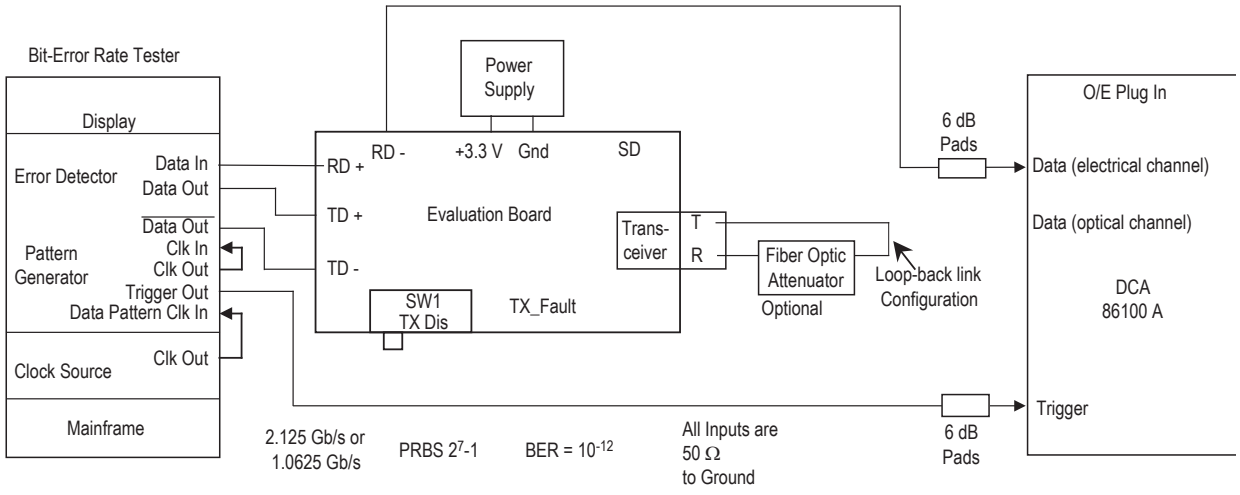

Figure 3. Recommended Receiver Configuration

Results

The following example measurements were made using the configurations illustrated in Figures 2 and 3 respectively.

IV. EEPROM Test Configuration

The SFP MSA specifies an EEPROM internal to the transceiver meeting the ATMEL AT24C01A industry standard specifications. The standard two-wire serial protocol can be implemented to allow the user to read the contents of the EEPROM by using the MOD_DEF (1) AND MOD_DEF(2) connections on the evaluation board. Note that MOD_DEF (0) is grounded by the module to indicate that the module is present and is not used during the read operation of the EEPROM.

A typical test configuration reading the EEPROM is illustrated in Figure 6. This configuration includes an optional EEPROM reader such as that from ChipMax and Control PC. This EEPROM reader uses a standard 40-pin Textool socket to interface to the device under test and a parallel port to interface to a control computer to utilize the software provided with the ChipMax unit. The textool socket is divided into slots for a 24-pin DIP and slots for an 8-pin DIP. The pins referenced in Figure 6 refer to the slots for the 8-pin DIP.

Information regarding pin definitions and contents for the EEPROM can be found in the specific Avago Technologies SFP module data sheets or by checking the SFP Multi-Source Agreement.

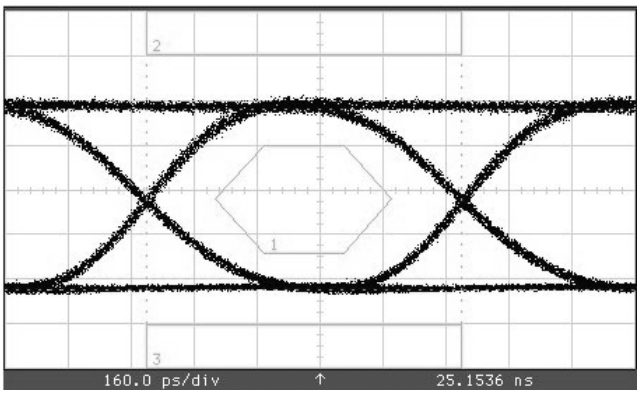

Figure 4. Example Transmitter Eye Diagram

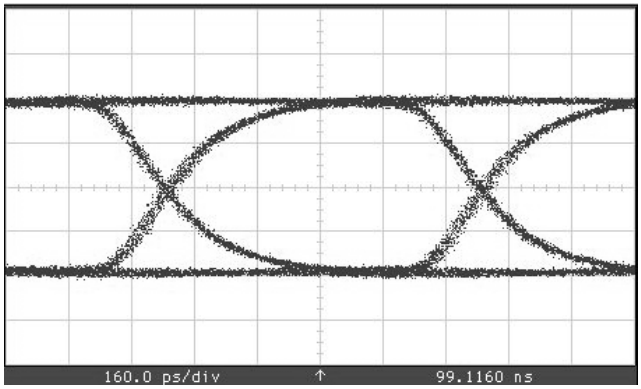

Figure 5. Example Loop Back Receiver Eye Diagram, -17 dBm power

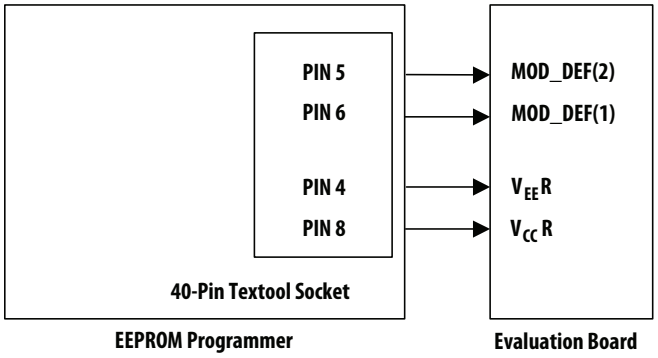

Figure 6. EEPROM Test Configuration

V. Evaluation Board Schematic and Bill of Materials

The SFP evaluation board electrical schematic is shown in Figure 7 at the end of this document. The user may notice connections on the board which are not represented on this schematic (Figure 7) or pin description (Table 1). This is due to optional functionality of the board. For simplicity and ease of application, only those connections and parts included are described in the schematic and bill of materials (Table 2).

VI. References

1. HFBR-57xx Product Data Sheets URL – **http://www.avagotech.com**
2. Avago Technologies Application Notes (AN) – **http://www.avagotech. com**
3. Small Form Factor Pluggable (SFP) Multisource Agreement – **http://www.avagotech. com**
4. Test Equipment User Manuals – **http://www.avagotech.com**

Table 2. SFP Evaluation Board Bill of Materials

Component	Type	Value	Footprint	Comments
PCB	SFP Evaluation Board			Unpopulated 4 layer circuit board
U1	Surface Mount socket (20 pin)			AMP 1367073-1
	Case jacks			0 (4 off), Advance Interconnect part 1718 or Cambion 450-3704-01-03-00
Q1	Transistor		UMX3N	Rohm dial NPN transistor, not included
	Device jacks			
	Nose jacks			0 (2 off), Cambion part 450-3704-01-03-00
R3, R5, R6, R7, R8	Resistor	4.7 kΩ	805	
C5, C7, C8, C10	Capacitor	0.1 μF	805	10% Tolerance
C6, C9	Capacitor	10 μF	Case code B	Tantalum 20% Tolerance
C13	Capacitor	10 μF	Case code B	Tantalum 20% Tolerance
L1, L2	Inductor	1 μF	1812	
SW1	Switch			Apem 25336NA
J1, J2, J3, J4	End launch SMA jack-tab contact			Johnson Components part number 142-0701-851
J5	Jack, 2 mm white			SD, Signal Detect
J8	Jack, 2 mm red			VccR
J9	Jack, 2 mm black			VeeR, RX_GND
J10	Jack, 2 mm white			TX_FAULT
J12, J13, J14	Jack, 2 mm white			MOD_DEF

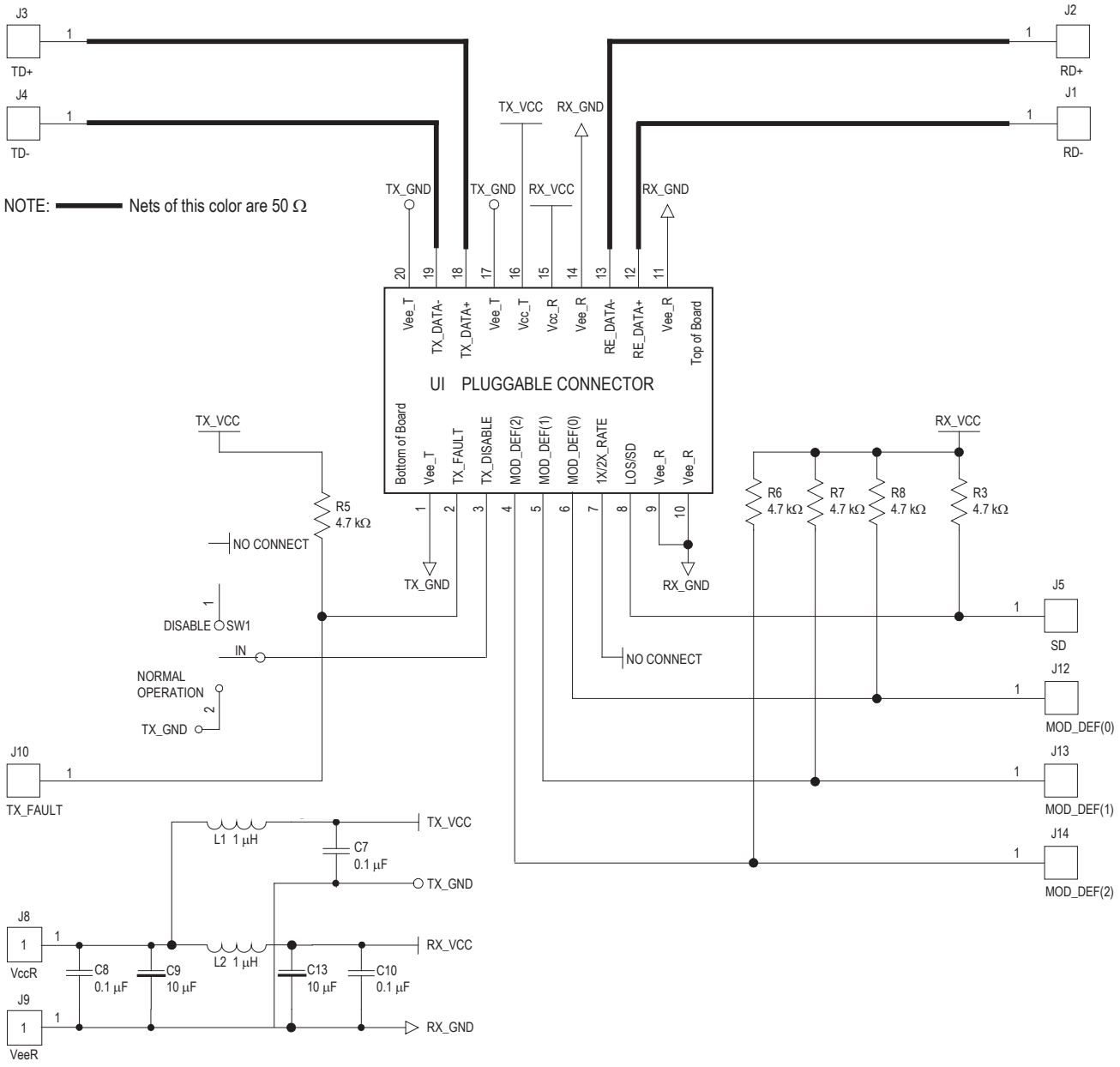

Figure 7. SFP Evaluation Board Circuit

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